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# PATENT APPLICATION

# METHOD OF MANUFACTURING NON-VOLATILE DRAM

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# METHOD OF MANUFACTURING NON-VOLATILE DRAM

## CROSS-REFERENCES TO RELATED APPLICATIONS

**[0001]** The present application claims benefit under 35 USC 119(e) of US provisional application number 60/540,885, filed on January 29, 2004, entitled "Method Of Manufacturing Non-Volatile Memory Device", Attorney Docket Number 021801-001100US, the content of which is incorporated herein by reference in its entirety.

## BACKGROUND OF THE INVENTION

**[0002]** The present invention relates to semiconductor integrated circuits. More particularly, the invention provides a semiconductor memory that has integrated non-volatile and dynamic random access memory cells. Although the invention has been applied to a single integrated circuit device in a memory application, there can be other alternatives, variations, and modifications. For example, the invention can be applied to embedded memory applications, including those with logic or micro circuits, and the like.

**[0003]** Semiconductor memory devices have been widely used in electronic systems to store data. There are generally two types of memories, including non-volatile and volatile memories. The volatile memory, such as a Static Random Access Memory (SRAM) or a Dynamic Random Access Memory (DRAM), loses its stored data if the power applied has been turned off. SRAMs and DRAMs often include a multitude of memory cells disposed in a two dimensional array. Due to its larger memory cell size, an SRAM is typically more expensive to manufacture than a DRAM. An SRAM typically, however, has a smaller read access time and a lower power consumption than a DRAM. Therefore, where fast access to data or low power is needed, SRAMs are often used to store the data.

**[0004]** Non-volatile semiconductor memory devices are also well known. A non-volatile semiconductor memory device, such as flash Erasable Programmable Read Only Memory (Flash EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM) or, Metal Nitride Oxide Semiconductor (MNOS), retains its charge even after the power applied thereto is turned off. Therefore, where loss of data due to power failure or termination is unacceptable, a non-volatile memory is used to store the data.

[0005] Unfortunately, the non-volatile semiconductor memory is typically slower to operate than a volatile memory. Therefore, where fast store and retrieval of data is required, the non-volatile memory is not typically used. Furthermore, the non-volatile memory often requires a high voltage, e.g., 12 volts, to program or erase. Such high voltages may cause a number of disadvantages. The high voltage increases the power consumption and thus shortens the lifetime of the battery powering the memory. The high voltage may degrade the ability of the memory to retain its charges due to hot-electron injection. The high voltage may cause the memory cells to be over-erased during erase cycles. Cell over-erase results in faulty readout of data stored in the memory cells.

[0006] The growth in demand for battery-operated portable electronic devices, such as cellular phones or personal organizers, has brought to the fore the need to dispose both volatile as well as non-volatile memories within the same portable device. When disposed in the same electronic device, the volatile memory is typically loaded with data during a configuration cycle. The volatile memory thus provides fast access to the stored data. To prevent loss of data in the event of a power failure, data stored in the volatile memory is often also loaded into the non-volatile memory either during the configuration cycle, or while the power failure is in progress. After power is restored, data stored in the non-volatile memory is read and stored in the volatile memory for future access. Unfortunately, most of the portable electronic devices may still require at least two devices, including the non-volatile and volatile, to carry out backup operations. Two devices are often required since each of the devices often rely on different process technologies, which are often incompatible with each other.

[0007] To increase the battery life and reduce the cost associated with disposing both non-volatile and volatile memory devices in the same electronic device, non-volatile SRAMs and non-volatile DRAMs have been developed. Such devices have the non-volatile characteristics of non-volatile memories, i.e., retain their charge during a power-off cycle, but provide the relatively fast access times of the volatile memories.

[0008] As merely an example, Fig. 1 is a transistor schematic diagram of a prior art non-volatile DRAM 10. Non-volatile DRAM 10 includes transistors 12, 14, 16 and EEPROM cell 18. The control gate and the drain of EEPROM cell 18 form the DRAM capacitor. Transistors 12 and 14 are parts of the DRAM cell. Transistor 16 is the mode selection

transistor and thus selects between the EEPROM and the DRAM mode. EEPROM cell 18 may suffer from the high voltage problems, is relatively large and thus is expensive.

**[0009]** Accordingly, a need continues to exist for a relatively small non-volatile DRAM that consumes less power than those in the prior art, does not suffer from read errors caused by over-erase, and is not degraded due to hot-electron injection.

**[0010]** While the invention is described in conjunction with the preferred embodiments, this description is not intended in any way as a limitation to the scope of the invention. Modifications, changes, and variations, which are apparent to those skilled in the art can be made in the arrangement, operation and details of construction of the invention disclosed herein without departing from the spirit and scope of the invention.

## BRIEF SUMMARY OF THE INVENTION

**[0011]** In accordance with the present invention, a method for making a non-volatile DRAM in a semiconductor substrate includes, in part, the steps of, forming at least two isolation regions in the semiconductor substrate, forming a well between the two isolation regions, where the well defines a body region, forming a first oxide layer above a first portion of the body region, forming a first dielectric layer above the first oxide layer, forming a first polysilicon layer above the first dielectric layer, wherein the first polysilicon layer forms a control gate of the non-volatile device of the non-volatile DRAM, forming a second dielectric layer above the first polysilicon layer, forming a first spacer above the body region and adjacent the first polysilicon layer, forming a second oxide layer above a second portion of the body region not covered by the first spacer, forming a second polysilicon layer over the second oxide layer, the first spacer and a portion of the second dielectric layer; wherein the second polysilicon layer forms a guiding gate of the non-volatile device of the non-volatile DRAM and a gate of an MOS transistor of the non-volatile DRAM, delivering first implants to the body region to form lightly doped areas in the body region, delivering second implants to the body region to define source and drain regions; forming a second spacer above the body region to define regions receiving lightly dopes implants and to define a conducting region of a capacitor of the non-volatile DRAM.

**[0012]** In some embodiments, the semiconductor substrate is a p-type substrate. In such embodiments, the first well is an p-well formed using a number of implant steps each using a different energy and doping concentration of Boron. Furthermore, in such embodiments, the

second well is an n-well formed using a number of implant steps each using a different energy and doping concentration of Phosphorous. In some embodiments, the implant steps used to form the n-well and p-well are carried out using a single masking step.

**[0013]** In some embodiments, the first dielectric layer further includes an oxide layer and a nitride layer and the second dielectric layer is a nitride-oxide layer. Moreover, the thickness of the second oxide layer is greater than that of the first oxide layer.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** Fig. 1 is a simplified transistor schematic diagram of a non-volatile DRAM, as known in the prior art.

**[0015]** Fig. 2 is a simplified transistor schematic diagram of a non-volatile DRAM, in accordance with one embodiment of the present invention.

**[0016]** Fig. 3 is a cross-sectional view of an embodiment of a non-volatile memory device disposed in the non-volatile DRAM of Fig. 2, in accordance with the present invention.

**[0017]** Fig. 4 is a cross-sectional view of a semiconductor substrate in which the non-volatile DRAM of Fig. 2 is formed.

**[0018]** Fig. 5 is a cross-sectional view of the semiconductor structure of Fig. 4 after a layer of pad oxide is formed thereon.

**[0019]** Fig. 6 is a cross-sectional view of the semiconductor structure of Fig. 5 after a layer of nitride is deposited on the pad oxide.

**[0020]** Fig. 7 is a cross-sectional view of the semiconductor structure of Fig. 6 after formation of trench isolation vias.

**[0021]** Fig. 8 is a cross-sectional view of the semiconductor structure of Fig. 7 after the trench isolations are filled with dielectric materials.

**[0022]** Fig. 9A is a cross-sectional view of the semiconductor structure of Fig. 8 after formation of a p-well defining a body region in which the non-volatile DRAM of Fig. 2 is formed.

**[0023]** Fig. 9B is a cross-sectional view of the semiconductor structure of Fig. 9A after formation of an n-well below the p-well.

**[0024]** Fig. 10 is a cross-sectional view of the semiconductor structure of Fig. 9 after a second n-well is formed adjacent the first n-well and p-well.

**[0025]** Fig. 11 is a cross-sectional view of the semiconductor structure of Fig. 10 after formation of various layers thereon.

**[0026]** Fig. 12 is a cross-sectional view of the semiconductor structure of Fig. 11 after a photo-resist mask has been formed to define the control gate of the non-volatile memory device.

**[0027]** Fig. 13 is a cross-sectional view of the semiconductor structure of Fig. 12 following etching steps and oxide spacer formation steps.

**[0028]** Fig. 14 is a cross-sectional view of the semiconductor structure of Fig. 13 after a second p-well a third n-well and various gate oxide layers have been formed.

**[0029]** Fig. 15A is a cross-sectional view of the semiconductor structure of Fig. 14 after a second poly layer has been deposited and photo-resist masks have been formed to define gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices, in accordance with a first embodiment.

**[0030]** Fig. 15B is a cross-sectional view of the semiconductor structure of Fig. 14 after a second poly layer has been deposited and photo-resist masks have been formed to define gate regions of high-voltage and low-voltage NMOS and PMOS transistors as well as the guiding gates of a pair of non-volatile devices, in accordance with a second embodiment.

**[0031]** Fig. 16A is a cross-sectional view of the semiconductor structure of Fig. 15A after various etching steps are carried out to form the gate regions of high-voltage and low-voltage NMOS and PMOS transistors, NMOS wordline pass gates, as well as the guiding gates of a pair of non-volatile devices.

**[0032]** Fig. 16B is a cross-sectional view of the semiconductor structure of Fig. 15B after various etching steps are carried out to form the gate regions of high-voltage and low-voltage NMOS and PMOS transistors, NMOS wordline pass gates, as well as the guiding gates of a pair of non-volatile devices.

**[0033]** Fig. 17A is a cross-sectional view of the semiconductor structure of Fig. 16A after a photo-resist mask has been formed to remove polysilicon stringers, oxide spacers and to define various LDD regions.

[0034] Fig. 17B is a cross-sectional view of the semiconductor structure of Fig. 16B after a photo-resist mask has been formed to remove exposed portions of polysilicon guiding gates, the underlaying oxide spacers and gate oxide layers.

[0035] Fig. 18 is a cross-sectional view of the semiconductor structure of Fig. 17A or 17B after removal of photo-resist masks and forming LDD regions.

[0036] Fig. 19 is a cross-sectional view of the semiconductor structure of Fig. 18 after formation of a second oxide spacer layer and performing source/drain implant regions.

[0037] Fig. 20 is a cross-sectional view of the semiconductor structure of Fig. 19 after formation of a Salicide layer.

[0038] Fig. 21 is a cross-sectional view of the semiconductor structure of Fig. 20 after deposition of insulating layers and deposition and patterning of a masking layer.

[0039] Fig. 22 is a cross-sectional view of the semiconductor structure of Fig. 21 after etching and deposition of an insulating layer.

[0040] Fig. 23 is a cross-sectional view of the semiconductor structure of Fig. 22 after formation sidewall spacers.

[0041] Fig. 24 is a cross-sectional view of the semiconductor structure of Fig. 23 after performing an etching step.

[0042] Fig. 25 is a cross-sectional view of the semiconductor structure of Fig. 24 after formation of the bit line and VPP.

## DETAILED DESCRIPTION OF THE INVENTION

[0043] According to the present invention, an improved memory device and method is provided. More particularly, the invention provides a semiconductor memory that has integrated non-volatile and Dynamic random access memory cells. Although the invention has been applied to a single integrated circuit device in a memory application, there can be other alternatives, variations, and modifications. For example, the invention can be applied to embedded memory applications, including those with logic or microcircuits, and the like.

[0044] Fig. 2 is a transistor schematic diagram of a non-volatile dynamic random access memory (DRAM) 50. DRAM 50 includes non-volatile device 52, as well as MOS transistor 54 and capacitor 56 which together form a dynamic random access memory cell, in

accordance with one embodiment of the present invention. This diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives.

**[0045]** Non-volatile DRAM (hereinafter alternatively referred to as memory) 50 includes 6 terminals, namely Cg, Cc, WL, BL, A, B. Memory 50 may be part of a memory array (not shown) disposed in a semiconductor Integrated Circuit (IC) adapted, among other functions, to store and supply the stored data. Terminals BL typically forms a bitline of such a memory array and terminal WL typically forms a wordline of such a memory array. In the following terminal BL is alternatively referred to as bitlines BL. In the following terminal WL is alternatively referred to as wordline WL.

**[0046]** The gate and drains terminals of MOS transistor 54 are respectively coupled to wordline WL and bitline BL. The source terminal of MOS transistor 54 is coupled to the source terminal of non-volatile device 52 via node N. Non-volatile memory device 52 has a guiding gate region and a control gate region. The guiding gate and control gate regions of non-volatile device 52 are respectively coupled to input terminals Cg and Cc of memory 50. The drain region of non-volatile device 52 is coupled to input terminal A of memory 50. The substrate (i.e., the bulk or body) region of non-volatile device 52 is coupled to input terminal B of memory 50.

**[0047]** Fig. 3 is a cross-sectional view of some of the regions of non-volatile memory device 52 (hereinafter alternatively referred to as device 52), in accordance with the present invention. Device 52 which is formed in, e.g., a p-type semiconductor substrate or a p-well formed in an n-type semiconductor substrate, includes, in part, a guiding gate 152a, a control gate 124, n-type source/drain regions 178 formed in p-well 114. Control gate 124, which is typically formed from polysilicon, is separated from p-type substrate or p-well layer 114 via oxide layer 118, nitride layer 120 and oxide layer 122. Guiding gate 152a, which is also typically formed from polysilicon, is separated from p-well 114 via oxide layer 134. Guiding gate 152a partially extends over control gate 124 and is separated therefrom via oxide-nitride layer 126. In the following, it is understood that similar elements or regions in the drawings are identified with similar reference numerals. Moreover, after various regions or elements in a drawing are identified with their respective reference numerals, the subsequent drawings may omit those reference numerals for simplification purposes.

[0048] As described above, transistor 54 together with the capacitance of node N form a DRAM cell. In the embodiment shown in Fig. 2, the capacitance at node N, i.e., capacitor 56, includes parasitic capacitances as well as actively formed capacitances. For example, capacitor 54 may be formed from layers of poly-silicon insulated from one another by a dielectric, e.g., silicon dioxide, layer. Described below is a method of manufacturing Non-volatile DRAM 50.

[0049] Fig. 4 shows a semiconductor substrate 100 in which non-volatile DRAM 50 shown in Fig. 2 is formed. In the exemplary embodiment described above, substrate 100 is a p-type substrate. It is understood that in other embodiments, substrate 100 may be an n-type substrate. To form non-volatile DRAM 50, a layer of pad oxide 102 having a thickness in the range of, e.g., 60-1000 Å, is grown on substrate 100 using conventional thermal oxidation processes, as shown in Fig. 5. Next, as shown in Fig. 6, a layer of silicon- nitride 104 having a thickness in the range of, e.g., 1000 Å, is deposited on pad oxide layer 102. It is understood that the various layers and spacings shown in the Figures are not drawn to scale. Next, using conventional masking and etching steps, shallow trenches 106 are formed in substrate 100, thereby forming structure 505 as shown in Fig. 7.

[0050] After shallow trenches 106 are formed, a layer of oxide having a thickness of, e.g., 150 Å, is grown over structure 505. This oxide is also grown in trenches 106. Next, a layer of TEOS having a thickness of, e.g., 5000-10,000 Å is deposited on the oxide. This TEOS is also deposited in trenches 106. Thereafter, using a planarization technique, such as chemical-mechanical polishing (CMP), the resulting structure is planarized. Fig. 8 shows the resulting structure 510 after the planarization process. As is seen from Fig. 8, as all the layers overlaying substrate 100, except for the oxide layer 108 and TEOS layer 110 formed in trenches 106, are removed.

[0051] Next, as shown in Figs. 9A and 9B using conventional photo-resist patterning and etching steps, p-well 114 and n-well 112 are formed using the same masking step. As seen from Fig. 9B, n-well 112 is deeper than and formed after p-well 114. In some embodiments, five separate Boron implants are used to form p-well implant 114. The first Boron implant is made using a concentration of $2.0e^{13}$ atoms/cm$^2$ and an energy of 600 Kilo-electron volts. The second Boron implant is made using a concentration of $1.0e^{13}$ atoms/cm$^2$ and an energy of 300 Kilo-electron volts. The third Boron implant is made using a concentration of $4.0e^{13}$ atoms/cm$^2$ and an energy of 160 Kilo-electron volts. The fourth Boron implant is made

using a concentration of $6.0e^{13}$ atoms/cm$^2$ and an energy of 70 Kilo-electron volts. The fifth Boron implant is made using a concentration of $1.0e^{13}$ atoms/cm$^2$ and an energy of 300 Kilo-electron volts. In such embodiments, a Phosphorous implant with a concentration of $2.0e^{13}$ atoms/cm$^2$ and using an energy of 1.5 Mega-electron volts is used to form n-well 112. AS described above, the above phosphorous and Boron implants are performed using the same masking step.

**[0052]** Because, the Phosphorous implant is performed using a relatively high energy, relatively few Phosphorous impurities may remain in p-well 114. Therefore, in accordance with the present invention, advantageously very few Boron impurities in p-well 114 are neutralized (i.e., compensated) by the phosphorous impurities.

**[0053]** Next, as shown in Fig. 10, a second n-well 116 is formed adjacent n-well 112 and p-well 114. N-well 116 that extends to the surface of substrate 100 has a depth that is substantially the same as the combined depth of n-well 112 and p-well 114. After the above implants, a rapid thermal anneal is performed at the temperature of, e.g., 1050 °C for a period of, e.g., 30 seconds. The resulting structure 520 is shown in Fig. 10 (also see Fig. 9B). As is seen from Fig. 10, n-well 116 and deep n-well 112 are connected in substrate 100.

**[0054]** Next, as shown in Fig. 11, a layer of thermal oxide 118 having a thickness in the range of, e.g., 15-50Å, is grown over structure 520. Thereafter, a layer of nitride 120 having a thickness in the range of, e.g., 40-120 Å , is formed over oxide layer 118. Next, a layer of CVD oxide 122 having a thickness in the range of, e.g., 40-70 Å, is deposited over nitride layer 120. Thereafter, during a densification step, the resulting structure is heated to a temperature of, e.g., 800 °C for a period of, e.g., 0.2 to 1 hour. After the densification step, a layer of polysilicon (alternatively referred to herein below as poly) 124 having a thickness in the range of, e.g., 1000-3000 Å is deposited over CVD oxide layer 122. Poly layer 124 may be doped in-situ or using other conventional doping techniques such as a ion implantation. Thereafter, a layer of insulator of nitride or oxide or combination layer 126 having a combined thickness in the range of, e.g., 500-1500 Å is formed over ploy layer 124. The thickness of oxide layer in the oxide-nitride layer 126 may be between, e.g., 500-1500 Å. Fig. 11 shows structure 525 that is formed after the above growth and deposition steps are performed on structure 520.

**[0055]** Next, using standard photo-resist deposition, patterning and etching steps, photo-resists masks 128 are formed over oxide-nitride layer 126. The resulting structure 530 is

shown in Fig. 12. Mask 128 is subsequently used to define the control gates of the non-volatile devices formed in substrate 100.

**[0056]** Next, using conventional etching techniques, such as reactive ion etching, all the various layers grown or deposited on substrate 100, namely layers 120, 122, 124 and 126 are removed from substantially all regions down to the surface of substrate 118 except for the regions positioned below masks 128. Thereafter, photo-resist masks 128 are also removed. Next, a layer of gate oxide 130 is thermally grown. In some embodiments, gate oxide layer 130 has a thickness in the range of, e.g., 100-200 Å. As is known to those skilled in the art, during this thermal oxidation, portions of polysilicon layer 124 are also oxidized, thereby causing the formation of rounded oxide regions 132, commonly referred to as spacers region. Structure 535 of Fig. 13 shows the result of performing these steps on structure 530. It is understood that the drawings do not show some of the intermediate steps involved in forming structure 535 from structure 530.

**[0057]** Next, using conventional anisotropic etching techniques, oxide layer 130 overlaying substrate 100 is removed as a result of which spacers 132 are also partially etched. Next, using conventional masking and ion implantation steps, highly doped p-well region 140 is formed (see Fig. 14). In some embodiments, four separate Boron implants are used to form p-well implant 140. The first Boron implant is made using a concentration of $3.3e^{12}$ atoms/cm$^2$ and an energy of 20 Kilo-electron volts (Kev). The second Boron implant is made using a concentration of $6.5e^{12}$ atoms/cm$^2$ and an energy of 70 Kev. The third Boron implant is made using a concentration of $3.4e^{12}$ atoms/cm$^2$ and an energy of 180 Kev. The fourth Boron implant is made using a concentration of $3.5e^{13}$ atoms/cm$^2$ and an energy of 500 Kilo-electron volts.

**[0058]** Next using conventional masking and ion implantation steps, highly doped n-well region 142 is formed (see Fig. 14). In some embodiments, four separate Phosphorous implants are used to form n-well implant 142. The first Phosphorous implant is made using a concentration of $5.7e^{12}$ atoms/cm$^2$ and an energy of 50 Kev. The second Phosphorous implant is made using a concentration of $6.6e^{12}$ atoms/cm$^2$ and an energy of 150 Kev. The third Phosphorous implant is made using a concentration of $5.0e^{12}$ atoms/cm$^2$ and an energy of 340 Kev. The fourth Phosphorous implant is made using a concentration of $4.0e^{13}$ atoms/cm$^2$ and an energy of 825 Kilo-electron volts. After the above implants, a thermal anneal is performed at the temperature of, e.g., 1000 °C for a period of, e.g., 10 seconds.

[0059] Thereafter using several masking steps, three layers of oxide thickness each having a different thickness are thermally grown. In the surface regions identified with reference numeral 134, the oxide layer has a thickness in the range of, e.g., 25-70 Å. The semiconductor substrate underlaying oxide layer 134 is used to form core transistors having relatively high speed. The semiconductor substrate underlaying oxide layer 138 and overlaying p-well 114 is used to form high-voltage transistors. In the region identified by reference numeral 138, the oxide layer has a thickness in the range of, e.g., 160-250 Å. The semiconductor substrate underlaying oxide layer 138 is used to form high-voltage transistors, such as Input/Output transistors. The process of making multiple, e.g. 3, layers of oxide each with a different thickness is known to those skilled in the art and is not described herein. Structure 540 of Fig. 14 shows the result of performing these steps on structure 535 of Fig. 13. It is understood that the drawings do not show some of the intermediate steps involved in forming structure 540 from structure 535.

[0060] Next, a layer of polysilicon 144 having a thickness in the range of, e.g., 1200-3200 Å, is deposited. Thereafter using standard photo-resist masking and patterning techniques, photo-resists masks 146 are formed over polysilicon layer 144. Structure 545A of Fig. 15A shows the result of performing these steps on structure 540 of Fig. 14, in accordance with the first embodiment. Structure 545B of Fig. 15B shows the result of performing these steps on structure 540 of Fig. 14, in accordance with the second embodiment. As is seen from the drawings, in contrast to Fig. 15B in which photo-resist masks 146 covers most of the surface area of each region in which non-volatile memory devices 52 are partly formed, photo-resist masks 146 in Fig. 15A cover only half the surface area of each region in which non-volatile memory devices 52 are partly formed.

[0061] Next, using conventional etching steps, polysilicon layer 144 are removed from all regions except those positioned below masks 146. Structure 550A of Fig. 16A shows the result of performing these steps on structure 545A of Fig. 15A, in accordance with the first embodiment. Structure 550B of Fig. 16B shows the result of performing these steps on structure 545B of Fig. 15B, in accordance with the second embodiment. Poly gate 148 is shown as overlaying gate oxide layer 134 formed above n-well 142. Poly gate 150 is shown as overlaying gate oxide layer 134 formed above p-well 140. Poly gates 152A and 152B are shown as overlaying gate oxide layer 134 formed above p-well 114. Poly gate 156 is shown as overlaying gate oxide layer 138 formed above n-well 116. Poly gates 148 and 150

respectively form the gates of low-voltage high-speed PMOS and NMOS transistors. Poly gate 156 forms the gate of a high-voltage PMOS transistor.

**[0062]** In accordance with the second embodiment 550B shown in Fig. 16B and as described further below, poly gates 152A and 152B are subjected to additional masking steps to form the guiding gates of a pair of non-volatile devices. Poly gates 152A and 152B of Fig. 16B are shown as fully overlaying gate oxide layer 134 and the oxide spacers of its associated non-volatile device. In accordance with the first embodiment shown in Fig. 16A, poly gates 152A and 152B respectively form the guiding gates of a pair of non-volatile devices and are shown as partly overlaying gate oxide layer 134 and one of the oxide spacers of its associated non-volatile device. Fig. 16A also shows poly stringers 153a and 153b that remain after the above etching steps are performed.

**[0063]** Next, using conventional photo-resist deposit and patterning techniques, photo-resist masks 158 are formed. Structure 555A of Fig. 17A shows the result of performing these steps on structure 550A of Fig. 16A, in accordance with the first embodiment. Structure 555B of Fig. 17B shows the result of etching the polysilicon on the vias 160A and 160B on structure 550B of Fig. 16B, in accordance with the second embodiment.

**[0064]** In accordance with the first embodiment, using either wet etching or plasma etching polysilicon stringers 153a and 153b exposed in vias 160A and 160B are removed from structure 555A. Thereafter, oxide spacers 132 and gate oxide layers 134 exposed in vias 160A and 160B are also removed. In accordance with the second embodiment, using either wet etching or reactive ion etching polysilicon layers 152A and 152B exposed in vias 160A and 160B are removed from structure 555B. Thereafter, oxide spacers 132 and gate oxide layers 134 in vias 160A and 160B are also removed. Next, using several masking steps, p-type lightly doped (LDD) regions 162, n-type LDD regions 164, n-type LDD regions 166, and p-type LDD region 170 are formed. Performing the above steps results in formation of structure 560 from either structure 555A or structure 555B. Accordingly, the steps described below apply to both embodiments and thus no distinction in the drawings is made hereinafter.

**[0065]** Next, as shown in Fig. 19, using conventional processing steps, side-wall spacers 172 are formed. In some embodiments, each side-wall spacer 172 is made from either oxide or nitride and each has a thickness in the rage of , e.g., 500-1500 Å. Thereafter, several $p^+$ and $n^+$ masking steps are performed to form $p^+$ source/drain regions 174, $n^+$ source/drain

regions 176, $n^+$ source/drain regions 178, and $p^+$ source/drain regions 180. In some embodiments, the doping concentration of Boron used to form $p^+$ source/drain regions 174 is the same as that used to form $p^+$ source/drain regions 180. In some other embodiments, the doping concentration of Boron used to form $p^+$ source/drain regions 174 is different from that used to form $p^+$ source/drain regions 180. In some embodiments, the doping concentration of Arsenic used to form $n^+$ source/drain regions 176 is the same as that used to form $n^+$ source/drain regions 178. In some other embodiments, the doping concentration of Arsenic used to form $n^+$ source/drain regions 176 is different from that used to form $n^+$ source/drain regions 178. The resulting structure 565 is shown in Fig. 19.

**[0066]** Next, a layer of metal such as Titanium or Tungsten is deposited over structure 565. Thereafter, a high-temperature anneal cycle is carried out. As is known to those skilled in the art, during the anneal cycle, the deposited metal reacts with silicon and polysilicon, but not with silicon-nitride or silicon-oxide. In the resulting structure 570, which is shown in Fig. 20, Salicided layers are identified with reference numeral 182. For simplicity, not all the layers are identified with reference numerals in Fig. 21 and subsequent Figures

**[0067]** Next, one or more layers 184 and 186 of insulating dielectric such as oxide, nitride or a combination thereof, is deposited over structure 570 and then patterned using conventional masking and etching steps to form vias 188, 190, 192, and 194. The patterned photo resist is identified in Fig. 21 with reference numeral 196. The resulting structure 575 is shown in Fig. 21.

**[0068]** Thereafter, photo resist 196 is removed and insulating layer 198 is deposited. The resulting structure 580 is shown in Fig. 22. Thereafter using known processing steps, insulating layer 198 and 186 and parts of insulating layer 184 are removed using reactive ion etching. This results in formation of sidewall spacers 184_A. The resulting structure 585 is shown in Fig. 23.

**[0069]** Next, salicide layer 182, polysilicon layers 152A, 152B, and oxide layer 134 are etched form areas adjacent sidewall spacers 184_A. Subsequently, LDD implants are carried out to form LDD regions 200. The resulting structure 590 is shown in Fig. 24.

**[0070]** Next, using standard processing steps, metal lines 216 and 218 are formed to make contacts with source/drain regions, as shown in Fig. 25. Metal line 216 is shown in Fig. 2 as

node A. Metal line 218 is shown in Fig. 2 as supply line Vpp. Non-volatile device cell 52 of Fig. 2 is identified in Fig. 24 with dashed perimeter line 52. Select transistor 54 of Fig. 2 is identified in Fig. 24 with dashed perimeter line 54. Storage capacitor 56 of Fig. 2 is identified in Fig. 24 with dashed perimeter line 56.

**[0071]** The above embodiments of the present disclosure are illustrative and not limitative. Other additions, subtractions, deletions, and modifications may be made without departing from the scope of the present invention as set forth in the appended claims.